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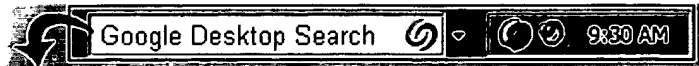
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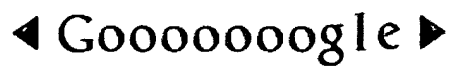
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## 1 [Massive arrays of idle disks for storage archives](#)

Dennis Colarelli, Dirk Grunwald

November 2002

**Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Full text available: [pdf\(751.87 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The declining costs of commodity disk drives is rapidly changing the economics of deploying large amounts of online or near-line storage. Conventional mass storage systems use either high performance RAID clusters, automated tape libraries or a combination of tape and disk. In this paper, we analyze an alternative design using *massive arrays of idle disks*, or MAID. We argue that this storage organization provides storage densities matching or exceeding those of tape libraries with perform ...

## 2 [Input/Output: Energy conservation techniques for disk array-based servers](#)

Eduardo Pinheiro, Ricardo Bianchini

June 2004

**Proceedings of the 18th annual international conference on Supercomputing**

Full text available: [pdf\(174.29 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we study energy conservation techniques for disk array-based network servers. First, we introduce a new conservation technique, called Popular Data Concentration (PDC), that migrates frequently accessed data to a subset of the disks. The goal is to skew the load towards a few of the disks, so that others can be transitioned to low-power modes. Next, we introduce a user-level file server that takes advantage of PDC. In the context of this server, we compare PDC to the Massive Array ...

**Keywords:** disk power, energy conservation, network servers

## 3 [DRPM: dynamic speed control for power management in server class disks](#)

Sudhanva Gurumurthi, Anand Sivasubramaniam, Mahmut Kandemir, Hubertus Franke

May 2003

**ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture, Volume 31 Issue 2**

Full text available: [pdf\(292.52 KB\)](#)

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A large portion of the power budget in server environments goes into the I/O subsystem - the disk array in particular. Traditional approaches to disk power management involve completely stopping the disk rotation, which can take a considerable amount of time, making them less useful in cases where idle times between disk requests may not be long enough to outweigh the overheads. This paper presents a new approach called DRPM to modulate disk speed (RPM) dynamically, and gives a practical impleme ...

**Keywords:** power management, server disks

## 4 [Power: Conserving disk energy in network servers](#)

Enrique V. Carrera, Eduardo Pinheiro, Ricardo Bianchini

June 2003

**Proceedings of the 17th annual international conference on Supercomputing**

Full text available: [pdf\(167.83 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper we study four approaches to conserving disk energy in high-performance network servers. The first approach is to leverage the extensive work on laptop disks and power disks down during periods of idleness. The second approach is to replace high-performance disks with a set of lower power disks that can achieve the same performance and reliability. The third approach is to combine high-performance and laptop disks, such that only one of these two sets of disks is powered on at a tim ...

**Keywords:** disk power, energy conservation, network servers

5 Input/Output: PB-LRU: a self-tuning power aware storage cache replacement algorithm for conserving disk energy

Qingbo Zhu, Asim Shankar, Yuanyuan Zhou

June 2004

**Proceedings of the 18th annual international conference on Supercomputing**

Full text available:  pdf(183.08\_KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Energy consumption is an important concern at data centers, where storage systems consume a significant fraction of the total energy. A recent study proposed power-aware storage cache management to provide more opportunities for the underlying disk power management scheme to save energy. However, the on-line algorithm proposed in that study requires cumbersome parameter tuning for each workload and is therefore difficult to apply to real systems. This paper presents a new power-aware on-line algo ...

**Keywords:** cache management, disk storage, power management

6 Reliability and security of RAID storage systems and D2D archives using SATA disk drives

Gordon F. Hughes, Joseph F. Murray

February 2005

**ACM Transactions on Storage (TOS)**, Volume 1 Issue 1

Full text available:  pdf(94.82\_KB)

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Information storage reliability and security is addressed by using personal computer disk drives in enterprise-class nearline and archival storage systems. The low cost of these serial ATA (SATA) PC drives is a tradeoff against drive reliability design and demonstration test levels, which are higher in the more expensive SCSI and Fibre Channel drives. This article discusses the tradeoff between SATA which has the advantage that fewer higher capacity drives are needed for a given system storage c ...


**Keywords:** Disk drive, SATA, SMART, archival storage, failure prediction, secure erase, storage resource management, storage systems architecture

7 Performance directed energy management for main memory and disks

Xiaodong Li, Zhenmin Li, Francis David, Pin Zhou, Yuanyuan Zhou, Sarita Adve, Sanjeev Kumar

October 2004

**Proceedings of the 11th international conference on Architectural support for programming languages and operating systems**, Volume 32 , 39 , 38 Issue 5 , 11 , 5

Full text available:  pdf(658.89\_KB)

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Much research has been conducted on energy management for memory and disks. Most studies use control algorithms that dynamically transition devices to low power modes after they are idle for a certain threshold period of time. The control algorithms used in the past have two major limitations. First, they require painstaking, application-dependent manual tuning of their thresholds to achieve energy savings without significantly degrading performance. Second, they do not provide performance guara ...

**Keywords:** adaptation algorithms, control algorithms, low power design, memory and disk energy management, multiple power mode device

8 Disk Drive Roadmap from the Thermal Perspective: A Case for Dynamic Thermal Management

Sudhanva Gurumurthi, Anand Sivasubramaniam, Vivek K. Natarajan

June 2005

**Proceedings of the 32nd Annual International Symposium on Computer Architecture ISCA '05**

Full text available:  pdf(243.57\_KB)

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The importance of pushing the performance envelope of disk drives continues to grow, not just in the server market but also in numerous consumer electronics products. One of the most fundamental factors impacting disk drive design is the heat dissipation and its effect on drive reliability, since high temperatures can cause off-track errors, or even head crashes. Until now, drive manufacturers have continued to meet the 40% annual growth target of the internal data rates (IDR) by increasing RPMs ...

9 An Efficient Data Location Protocol for Self-organizing Storage Clusters

Hong Tang, Tao Yang

November 2003

**Proceedings of the 2003 ACM/IEEE conference on Supercomputing**

Full text available:  pdf(345.61\_KB)

Additional Information: [full citation](#), [abstract](#)

Component additions and failures are common for large-scale storage clusters in production environments. To improve availability and manageability, we investigate and compare data location schemes for a large self-organizing storage cluster that can quickly adapt to the additions or departures of storage nodes. We further present an efficient location scheme that differentiates between small and large file blocks for reduced management overhead compared to uniform strategies. In our protocol, sm ...

10

An evaluation of redundant arrays of disks using an Amdahl 5890

Recently we presented several disk array architectures designed to increase the data rate and I/O rate of supercomputing applications, transaction processing, and file systems [Patterson 88]. In this paper we present a hardware performance measurement of two of these architectures, mirroring and rotated parity. We see how throughput for these two architectures is affected by response time requirements, request sizes, and read to write ratios. We find that for applications with large ...

**11 RAID: high-performance, reliable secondary storage**

Peter M. Chen, Edward K. Lee, Garth A. Gibson, Randy H. Katz, David A. Patterson

June 1994

**ACM Computing Surveys (CSUR)**, Volume 26 Issue 2

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Disk arrays were proposed in the 1980s as a way to use parallelism between multiple disks to improve aggregate I/O performance. Today they appear in the product lines of most major computer manufacturers. This article gives a comprehensive overview of disk arrays and provides a framework in which to organize current and future work. First, the article introduces disk technology and reviews the driving forces that have popularized disk arrays: performance and reliability. It discusses the tw ...


**Keywords:** RAID, disk array, parallel I/O, redundancy, storage, striping

**12 Destage algorithms for disk arrays with non-volatile caches**

Anujan Varma, Quinn Jacobson

May 1995

**ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2

Full text available:  pdf(1.63 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


In a disk array with a nonvolatile write cache, destages from the cache to the disk are performed in the background asynchronously while read requests from the host system are serviced in the foreground. In this paper, we study a number of algorithms for scheduling destages in a RAID-5 system. We introduce a new scheduling algorithm, called *linear threshold scheduling*, that adaptively varies the rate of destages to disks based on the instantaneous occupancy of the write cache. The perform ...

**13 Designing computer systems with MEMS-based storage**

Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger

November 2000

**Proceedings of the ninth international conference on Architectural support for programming languages and operating systems**, Volume 34 , 28 Issue 5 , 5

Full text available:  pdf(439.06 KB)

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For decades the RAM-to-disk memory hierarchy gap has plagued computer architects. An exciting new storage technology based on microelectromechanical systems (MEMS) is poised to fill a large portion of this performance gap, significantly reduce system power consumption, and enable many new applications. This paper explores the system-level implications of integrating MEMS-based storage into the memory hierarchy. Results show that standalone MEMS-based storage reduces I/O stall times by 4-74X over ...

**14 Designing computer systems with MEMS-based storage**

Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger

November 2000

**ACM SIGPLAN Notices**, Volume 35 Issue 11

Full text available:  pdf(439.06 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

For decades the RAM-to-disk memory hierarchy gap has plagued computer architects. An exciting new storage technology based on microelectromechanical systems (MEMS) is poised to fill a large portion of this performance gap, significantly reduce system power consumption, and enable many new applications. This paper explores the system-level implications of integrating MEMS-based storage into the memory hierarchy. Results show that standalone MEMS-based storage reduces I/O stall times by 4--74X ove ...

**15 An analytic performance model of disk arrays**

Edward K. Lee, Randy H. Katz

June 1993

**ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1993 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 21 Issue 1

Full text available:  pdf(1.13 MB)

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As disk arrays become widely used, tools for understanding and analyzing their performance become increasingly important. In particular, performance models can be invaluable in both configuring and designing disk arrays. Accurate analytic performance models are preferable to other types of models because they can be quickly evaluated, are applicable under a wide range of system and workload parameters, and

can be manipulated by a range of mathematical techniques. Unfortunately, analytic performa ...

16 File server scaling with network-attached secure disks

Garth A. Gibson, David F. Nagle, Khalil Amiri, Fay W. Chang, Eugene M. Feinberg, Howard Gobioff, Chen Lee, Berend Ozceri, Erik Riedel, David Rochberg, Jim Zelenka

June 1997

**ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems, Volume 25 Issue 1**

Full text available:  pdf(1.77 MB)

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By providing direct data transfer between storage and client, network-attached storage devices have the potential to improve scalability for existing distributed file systems (by removing the server as a bottleneck) and bandwidth for new parallel and distributed file systems (through network striping and more efficient data paths). Together, these advantages influence a large enough fraction of the storage market to make commodity network-attached storage feasible. Realizing the technology's ful ...

17 Comparing rebuild algorithms for mirrored and RAID5 disk arrays

Robert Y. Hou, Yale N. Patt

June 1993

**ACM SIGMOD Record , Proceedings of the 1993 ACM SIGMOD international conference on Management of data, Volume 22 Issue 2**

Full text available:  pdf(945.10 KB)

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Several disk array architectures have been proposed to provide high throughput for transaction processing applications. When a single disk in a redundant array fails, the array continues to operate, albeit in a degraded mode with a corresponding reduction in performance. In addition, the lost data must be rebuilt to a spare disk in a timely manner to reduce the probability of permanent data loss. Several researchers have proposed and examined algorithms for rebuilding the failed dis ...

18 Failure correction techniques for large disk arrays

G. A. Gibson, L. Hellerstein, R. M. Karp, D. A. Patterson

April 1989

**ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems, Volume 17 Issue 2**

Full text available:  pdf(1.24 MB)

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The ever increasing need for I/O bandwidth will be met with ever larger arrays of disks. These arrays require redundancy to protect against data loss. This paper examines alternative choices for encodings, or codes, that reliably store information in disk arrays. Codes are selected to maximize mean time to data loss or minimize disks containing redundant data, but are all constrained to minimize performance penalties associated with updating information or recovering from catastrophe ...

19 Asynchronous scheduling of redundant disk arrays

Peter Sanders

July 2000

**Proceedings of the twelfth annual ACM symposium on Parallel algorithms and architectures**

Full text available:  pdf(161.35 KB)

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Random redundant allocation of data to parallel disk arrays can be exploited to achieve low access delays. New algorithms are proposed which improve the previously known shortest queue algorithm by systematically exploiting that scheduling decisions can be deferred until a block access is actually started on a disk. These algorithms are also generalized for coding schemes with low redundancy. Using extensive experiments, practically important quantities are measured which have so far eluded ...

20 Performance of a disk array prototype

Ann L. Chervenak, Randy H. Katz

April 1991

**ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1991 ACM SIGMETRICS conference on Measurement and modeling of computer systems, Volume 19 Issue 1**

Full text available:  pdf(1.05 MB)

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The RAID group at U.C. Berkeley recently built a prototype disk array. This paper examines the performance limits of each component of the array using SCSI bus traces, Sprite operating system traces and user programs. The array performs successfully for a workload of small, random I/O operations, achieving 275 I/Os per second on 14 disks before the Sun4/280 host becomes CPU-limited. The prototype is less successful in delivering high throughput for large, sequential operations. Memory system cont ...

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## 1 [Reliability and security of RAID storage systems and D2D archives using SATA disk drives](#)

Gordon F. Hughes, Joseph F. Murray

February 2005 **ACM Transactions on Storage (TOS)**, Volume 1 Issue 1

Full text available: pdf(94.82 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Information storage reliability and security is addressed by using personal computer disk drives in enterprise-class nearline and archival storage systems. The low cost of these serial ATA (SATA) PC drives is a tradeoff against drive reliability design and demonstration test levels, which are higher in the more expensive SCSI and Fibre Channel drives. This article discusses the tradeoff between SATA which has the advantage that fewer higher capacity drives are needed for a given system storage c ...

**Keywords:** Disk drive, SATA, SMART, archival storage, failure prediction, secure erase, storage resource management, storage systems architecture

## 2 [DRPM: dynamic speed control for power management in server class disks](#)

Sudhanva Gurumurthi, Anand Sivasubramaniam, Mahmut Kandemir, Hubertus Franke

May 2003 **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture**, Volume 31 Issue 2

Full text available: pdf(292.52 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

A large portion of the power budget in server environments goes into the I/O subsystem - the disk array in particular. Traditional approaches to disk power management involve completely stopping the disk rotation, which can take a considerable amount of time, making them less useful in cases where idle times between disk requests may not be long enough to outweigh the overheads. This paper presents a new approach called DRPM to modulate disk speed (RPM) dynamically, and gives a practical impleme ...

**Keywords:** power management, server disks

## 3 [Massive arrays of idle disks for storage archives](#)

Dennis Colarelli, Dirk Grunwald

November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Full text available: pdf(751.87 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The declining costs of commodity disk drives is rapidly changing the economics of deploying large amounts of online or near-line storage. Conventional mass storage systems use either high performance RAID clusters, automated tape libraries or a combination of tape and disk. In this paper, we analyze an alternative design using *massive arrays of idle disks*, or MAID. We argue that this storage organization provides storage densities matching or exceeding those of tape libraries with perform ...

## 4 [Input/Output: Energy conservation techniques for disk array-based servers](#)

Eduardo Pinheiro, Ricardo Bianchini

June 2004 **Proceedings of the 18th annual international conference on Supercomputing**

Full text available: pdf(174.29 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we study energy conservation techniques for disk array-based network servers. First, we introduce a new conservation technique, called Popular Data Concentration (PDC), that migrates frequently accessed data to a subset of the disks. The goal is to skew the load towards a few of the disks, so that others can be transitioned to low-power modes. Next, we introduce a user-level file server that takes advantage of PDC. In the context of this server, we compare PDC to the Massive Array ...

**Keywords:** disk power, energy conservation, network servers

5 Power: Conserving disk energy in network servers

Enrique V. Carrera, Eduardo Pinheiro, Ricardo Bianchini

June 2003

**Proceedings of the 17th annual international conference on Supercomputing**

Full text available:  pdf(167.83 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper we study four approaches to conserving disk energy in high-performance network servers. The first approach is to leverage the extensive work on laptop disks and power disks down during periods of idleness. The second approach is to replace high-performance disks with a set of lower power disks that can achieve the same performance and reliability. The third approach is to combine high-performance and laptop disks, such that only one of these two sets of disks is powered on at a time ...

**Keywords:** disk power, energy conservation, network servers

6 Input/Output: PB-LRU: a self-tuning power aware storage cache replacement algorithm for conserving disk energy

Qingbo Zhu, Asim Shankar, Yuanyuan Zhou

June 2004

**Proceedings of the 18th annual international conference on Supercomputing**

Full text available:  pdf(183.08 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Energy consumption is an important concern at data centers, where storage systems consume a significant fraction of the total energy. A recent study proposed power-aware storage cache management to provide more opportunities for the underlying disk power management scheme to save energy. However, the on-line algorithm proposed in that study requires cumbersome parameter tuning for each workload and is therefore difficult to apply to real systems. This paper presents a new power-aware on-line algo ...

**Keywords:** cache management, disk storage, power management

7 Performance directed energy management for main memory and disks

Xiaodong Li, Zhenmin Li, Francis David, Pin Zhou, Yuanyuan Zhou, Sarita Adve, Sanjeev Kumar

October 2004

**Proceedings of the 11th international conference on Architectural support for programming languages and operating systems**, Volume 32 , 39 , 38 Issue 5 , 11 , 5

Full text available:  pdf(658.89 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Much research has been conducted on energy management for memory and disks. Most studies use control algorithms that dynamically transition devices to low power modes after they are idle for a certain threshold period of time. The control algorithms used in the past have two major limitations. First, they require painstaking, application-dependent manual tuning of their thresholds to achieve energy savings without significantly degrading performance. Second, they do not provide performance guara ...

**Keywords:** adaptation algorithms, control algorithms, low power design, memory and disk energy management, multiple power mode device

8 Disk Drive Roadmap from the Thermal Perspective: A Case for Dynamic Thermal Management

Sudhanva Gurumurthi, Anand Sivasubramaniam, Vivek K. Natarajan

June 2005

**Proceedings of the 32nd Annual International Symposium on Computer Architecture ISCA '05**

Full text available:  pdf(243.57 KB)

Additional Information: [full citation](#), [abstract](#)

The importance of pushing the performance envelope of disk drives continues to grow, not just in the server market but also in numerous consumer electronics products. One of the most fundamental factors impacting disk drive design is the heat dissipation and its effect on drive reliability, since high temperatures can cause off-track errors, or even head crashes. Until now, drive manufacturers have continued to meet the 40% annual growth target of the internal data rates (IDR) by increasing RPMs ...

9 An Efficient Data Location Protocol for Self-organizing Storage Clusters

Hong Tang, Tao Yang

November 2003

**Proceedings of the 2003 ACM/IEEE conference on Supercomputing**

Full text available:  pdf(345.61 KB)

Additional Information: [full citation](#), [abstract](#)

Component additions and failures are common for large-scale storage clusters in production environments. To improve availability and manageability, we investigate and compare data location schemes for a large self-organizing storage cluster that can quickly adapt to the additions or departures of storage nodes. We further present an efficient location scheme that differentiates between small and large file blocks for reduced management overhead compared to uniform strategies. In our protocol, sm ...

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Energy conservation for mobile devices: Ghosts in the machine: interfaces for better power



We observe that the modularity of current power management algorithms often leads to poor results. We propose two new interfaces that pierce the abstraction barrier that inhibits device power management. First, an OS power manager allows applications to query the current power mode of I/O devices to evaluate the performance and energy cost of alternative strategies for reading and writing data. Second, we allow applications to disclose *ghost hints* that enable better power management in th ...

**Keywords:** adaptive caching, energy-awareness, power management

**11 Channelization: A single-channel solution for transmission power control in wireless ad hoc networks**

Alaa Muqattash, Marwan Krunz

May 2004

**Proceedings of the 5th ACM international symposium on Mobile ad hoc networking and computing**

Full text available:  pdf(251.45 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Transmission power control (TPC) has a great potential to increase the throughput of a mobile ad hoc network (MANET). Existing TPC schemes achieve this goal by using additional hardware (e.g., multiple transceivers), by compromising the collision avoidance property of the channel access scheme, or by imposing impractical requirements on the operation of the MAC protocol. In this paper, we present a novel power control MAC protocol, known as POWMAC, for MANETs that enjoys the same simple single-c ...

**Keywords:** IEEE 802.11, ad hoc networks, interference margin, load control, multi-access interference, power control, throughput enhancement

**12 A knowledge-based approach for power system dynamic security assessment**

B. Jeyasurya, S. S. Venkata

June 1990

**Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2**

Full text available:  pdf(623.30 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents a knowledge-based method for predicting the robustness of a power system to severe disturbances. The method builds decision trees using the attributes which are closely related to the stability of the power system. A simple power system is used to illustrate the important features of the proposed method.

**13 Poster session 2: Cycle-accurate power analysis for multiprocessor systems-on-a-chip**

Mirko Loghi, Massimo Poncino, Luca Benini

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available:  pdf(191.54 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Developing energy-aware software for multiprocessor systems-on-chip (MPSoCs) is a difficult task, which requires the knowledge of the distribution of the power consumption among several heterogeneous devices (cores, memories, busses, etc.). In this work we analyze the power breakdowns of power consumption for a complete MPSoC platform, under several application workloads and operating conditions. We leverage a complete-system simulation platform with accurate power models for all key hardware mo ...

**Keywords:** low power, multiprocessor, system-on-chip

**14 Poster session 2: Low power ATPG for path delay faults**

M.M Vaseekar Kumar, S. Padmanaban, S. Tragoudas

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available:  pdf(186.91 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper we propose an implicit test pattern generation method so that many path delay faults are covered and the dissipated power satisfies a given bound. Typical delay values are considered from an accurate gate delay model. We use a timed ATPG that combines function-based and structural (PODEM-like) methods for faster test generation, which is also more accurate in sequential circuits.

**Keywords:** ATPG, PODEM, low power, path delay faults

**15 Low Power: Power macromodeling of global interconnects considering practical repeater insertion**

Yuantao Peng, Xun Liu

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

In this paper, we present a simple yet highly effective power macromodeling technique for global interconnects that considers optimal repeater insertion. Specifically, our model estimates the interconnect power dissipation from the interconnect length, the timing budget, the repeater location flexibility, and the signal activity using an analytical function that is derived for a given repeater library and fabrication technology. In experiments with different standard cell libraries, the average e ...

**Keywords:** interconnect, low power, macromodeling, repeater insertion

**16** Low Power: Mitigating static power in current-sensed interconnects

Vishak Venkatraman, Atul Maheshwari, Wayne Burleson

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available:  pdf(144.24 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Interconnects are an increasing concern in recent years, resulting in novel techniques such as current sensing. However these techniques must be designed to tradeoff delay and both dynamic and static power consumption. This paper presents an innovative approach to reduce static power in differential current-sensed interconnects. This system uses a self-timed shut-off system to reduce static currents used to bias the current sense amplifier. Results indicated that the self timed shut-off system r ...

**Keywords:** interconnect circuits, self-timed systems, static power

**17** Poster Session 1: FIFO power optimization for on-chip networks

Sudarshan Banerjee, Nikil Dutt

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available:  pdf(105.29 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

As the design community moves towards architecting multiprocessor systems-on-chip (MPSoC), it is widely believed that an on-chip interconnection network is potentially the best candidate to satisfy the high aggregate throughput needed by dozens of IP blocks. In this context, power (energy) estimation and reduction techniques for switches and links, the core components of an interconnection network, gain added significance. FIFO buffers are a key component of a majority of network switches - buff ...

**Keywords:** FIFO, low power design, on-chip networks, shared memory, switches, wide flits

**18** Poster Session 1: Leakage power minimization for the synthesis of parallel multiplier circuits

Keoncheol Shin, Taewhan Kim

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available:  pdf(775.85 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#), [review](#)

This paper presents a new approach to the synthesis of parallel multiplier circuits with an objective of minimizing leakage power consumption under circuit timing constraint. Our leakage power optimization is based on the use of dual-threshold voltage ( $V_t$ ) technology. From experiments using a set of benchmark designs, it is shown that the approach is quite effective.

**Keywords:** power optimization, synthesis

**19** Poster Session 1: Macro-models for high level area and power estimation on FPGAs

Tianyi Jiang, Xiaoyong Tang, Prith Banerjee

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available:  pdf(261.20 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

As more and more complex applications are implemented on FPGAs, high-level design tools are needed to reduce the design time. A good high-level synthesis tool usually has an automated design space exploration pass to determine the effects of various compiler optimizations on the area and power of the synthesized hardware. Such a pass needs early estimation of area and power. Towards this end, we have developed high-level equation based area and power macro-models for various RTL level operators ...

**Keywords:** FPGA, RTL, area estimation, high-level synthesis, model, power estimation

**20** CAD: High level techniques for power-grid noise immunity

Azadeh Davoodi, Vishal Khandelwal, Ankur Srivastava

April 2004

**Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available:  pdf(198.32 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Power-grid networks are very important aspects of large scale integrated systems. In the modern deep sub-micron era these networks are prone to many sources of noise hence making the voltage supply fluctuate. This Vdd-Ground noise can have detrimental effect on design quality. This paper presents a unique strategy of achieving noise immunity through voltage scheduling in Data Flow Graphs (DFGs). A dynamic programming based approach is applied to obtain noise immunity by imposing a grid on the volt ...

**Keywords:** high-level noise-immune optimization

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